

Publications

Matsuura, M., Sasao, T., Butler, J.T., and Iguchi, Y., "Bi-partition of Shared Binary Decision Diagrams", *Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI-2001)*, Nara, Japan, Oct 18-19, 2001, pp. 172-177.

Sasao, T. and Butler, J.T., "Worst and Best Sum-of-Products Expressions", *IEEE Transactions on Computers*, Sep 2001, pp. 935-948.

Butler, J.T., Dueck, G.W., Yanushkevich, S.N., and Shmerko, V.P., "On the Number of Generators for Transeunt Triangles," *Discrete Applied Mathematics*, 108, 2001, pp. 309-316.

Sasao, T. and Butler, J.T., "On the Minimization of SOPs for Bi-Decomposable Functions," *ASP-DAC (Asian So. Pacific Design Automation Conf.)*, Yokohama, Japan, Feb 2001, pp. 219-224.

Butler, J.T., Dueck, G.W., Shmerko, V.P., and Yanushkevich, S.N., "Comments on 'Fast Exact Minimization of Fixed Polarity Reed-Muller Expansion for Symmetric Functions'," *IEEE Trans. On Computer-Aided Design*, Vol 19, No. 11, Nov 2000, pp. 1386-1388.

Yanushkevich, S.V., Butler, J.T., Dueck, G.W., and Shmerko, V., "Experiments on FPRM Expressions for Partially Symmetric Logic Functions," *Proc. Of the 30th Inter. Symposium on Multiple-Valued Logic*, May 2000, pp. 141-146.

Butler, J.T., Dueck, G.W., Holowinski, G., Shmerko, V.P., and Yansushkevich, S.N., "Recognition of Symmetries for Switching Functions in Reed-Muller Forms," *Proc. Of the 5th Inter. Conf. On Pattern Recognition an Information Processing*, May 1999, pp. 215-234.

J. T. Butler and T. Sasao, "On the properties of multiple-valued functions that are symmetric in both variable values and labels," *Proceedings of the 28th International Symposium on Multiple-Valued Logic*, May 1998, pp. 83-88.

T. Sasao nd J. T. Butler, "Comparison of the worst and best sum-of-products expressions for multiple-valued functions," *Proceedings of the 27th International Symposium on Multiple-Valued Logic*, May 1997, pp. 55-60.

J. T. Butler and T. Sasao, "On the proportion of digits in redundant numeration systems," *The Fibonacci Quarterly*, May 1997, pp. 172-180.

J. T. Butler, D.S. Herscovici, T. Sasao, and R.J. Barton, "Average and worst case number of nodes in decision diagrams of symmetric multiple-valued functions," *IEEE Transactions on Computers*, April 1997, pp. 491-494.

K.A. Schueller and J. T. Butler, "Complexity analysis of the cost-table approach to the design of multiple-valued logic circuits," *IEEE Transactions on Computersebruary* 1997, pp. 205-209.

J. T. Butler and T. Sasao, "Average number of nodes in binary decision diagrams of Fibonacci functions", *The Fibonacci Quarterly*, Vol. 34.5, November 1996, pp. 413-422.

T. Sasao and J. T. Butler, "Planar decision diagrams for multiple-valued functions," *Multiple-Valued Logic: An International Journal* (inaugural issue - invited paper), Vol. 1., 1996, pp. 39-64. This is an extended version of a paper in the *Proceedings of the 25th International Symposium on Multiple-Valued Logic*.

Butler, J. L Nowlin and T. Sasao, "Planarity in ROMDD's of multiple-valued symmetric functions," *Proceedings of the 26th International Symposium on Multiple-Valued Logic*, May 1996, pp. 236-241.

T. Sasao and J. T. Butler, "Method to represent multiple-output switching functions by using multi-valued decision diagrams", *Proceedings of the 26th International Symposium on Multiple-Valued Logic*, May 1996, pp. 248-254.

G.W. Dueck and J. T. Butler, "A heat-quench algorithm for the minimization of multiple-valued programmable logic arrays", *Computer and Electrical Engineering Journal* Vol. 22, No. 2, 1996, pp. 103-107.

T. Sasao and J. T. Butler, "Planar multiple-valued decision diagrams", *Proceedings of the 25th International Symposium on Multiple-Valued Logic*, May 1995, pp. 28-35.

J. T. Butler, "Multiple-valued logic in ultra-high speed computation," *IEEE Potentials*, April/May 1995, April/May 1995 .

J. T. Butler and T. Sasao, "Multiple-valued combinational circuits with feedback," *Proceedings of the 24th International Symposium on Multiple-Valued Logic*, May 1994, pp. 342-347.

T. Sasao and J. T. Butler, "A decision method for look-up table type FPGA by pseudo-Kronecker expansion," *Proceedings of the 24th International Symposium on Multiple-Valued Logic*, May 1994, pp. 97-106.

G. W. Dueck and J. T. Butler, "Multiple-valued operations with universal literals," *Proceedings of the 24th International Symposium on Multiple-Valued Logic*, May 1994, pp. 73-79.

C. Yildirim and J. T. Butler and C. Yang, "Multiple-valued PLA minimization by concurrent multiple and mixed simulated annealing," *Proceedings of the 23rd International Symposium on Multiple-Valued Logic*, May 1993, pp. 17-23.

G. W. Dueck and J. T. Butler, "A minimization algorithm for non-concurrent PLA's," *International Journal of Electronics*, Vol. 73, No. 6, Dec. 1992, pp. 1113-1119.

G. W. Dueck, R. C. Earle, P. T. Tirumalai, and J. T. Butler, "Multiple-valued programmable logic array minimization by simulated annealing," *Proceedings of the 22nd International Symposium on Multiple-Valued Logic*, May 1992, pp. 66-74.

S. W. Butler and J. T. Butler, "Profiles of topics and authors of the International Symposium on Multiple-Valued Logic for 1971-91," *Proceedings of the 22nd International Symposium on Multiple-Valued Logic*, May 1992, pp. 372-381.

K. A. Schueller and J. T. Butler, "On the design of cost-tables for realizing multiple-valued circuits," *IEEE Transactions on Computers*, Vol. 41, No. 2, February 1992, pp. 178-189.

Y.H. Chang and J. T. Butler, "The design of current-mode CMOS multiple-valued circuits," *Proceedings of the 21st International Symposium on Multiple-Valued Logic*, May 1991, pp. 130-138.

J. T. Butler and K.A. Schueller, "Worst case number of terms in symmetric multiple-valued functions," *Proceedings of the 21st International Symposium on Multiple-Valued Logic*, May 1991, pp. 94-101.

P. P. Tirumalai and J. T. Butler, "Minimization algorithms for multiple-valued programmable logic arrays," *IEEE Transactions on Computers*, 1991, pp. 167-177; this is an extended version of P. P. Tirumalai and J. T. Butler, "Analysis of minimization algorithms for multiple-valued programmable logic arrays," *Proceedings of the 1988 International Symposium on Multiple-Valued Logic*, May 1988, pp. 272-279.

J. T. Butler, "On the number of propagation paths in multi-layer media," *Fibonacci Quarterly*, Vol. 28, No. 4, November 1990, pp. 334-339.

J.-k. Lee and J. T. Butler, "A characterization of t/s-diagnosability and sequential t-diagnosability in designs", *IEEE Transactions on Computers*, C-39, October 1990, pp. 1298-1304.

J. T. Butler and K.A. Schueller, "On the equivalence of cost functions in the design of circuits by cost-tables", *IEEE Transactions on Computers*, C39, June 1990, pp. 842-845.

J. Yurchak and J. T. Butler, "HAMLET - An expression compiler/optimizer for the implementation of heuristics to minimize multiple-valued programmable logic arrays", *Proceedings of the 20th International Symposium on Multiple-Valued Logic*, May 1990, pp. 144-152.

J. T. Butler and H.G. Kerkhoff and S. Onneweer, "A Comparative analysis of multiplexer techniques for the minimization of function cost using the cost-table approach",

Proceedings of the 20th International Symposium on Multiple-Valued Logic, May 1990, pp. 286-291.

H. G. Kerkhoff and J. T. Butler, "Module compiler for high-radix CCD-PLA's", *International Journal of Electronics*, Vol. 67, No. 5, November 1989, pp. 797-805.

P. Tirumalai and J. T. Butler, "Prime and nonprime implicants in the minimization of multiple-valued logic functions", *Proceedings of the 19th International Symposium on Multiple-Valued Logic*, May 1989, pp. 272-279.

E. A. Bender and J. T. Butler, "On the size of PLA's required to realize binary and multiple-valued functions," *IEEE Transactions on Computers*, C-38, Jan. 1989, pp. 82-98.

P. Tirumalai and J. T. Butler, "Analysis of minimization algorithms for multiple-valued programmable logic arrays," *Proceedings of the 18th International Symposium on Multiple-Valued Logic*, May 1988, pp. 226-236.

S. Onneweer, H. G. Kerkhoff, and J. T. Butler, "Structural computer-aided design of current-mode CMOS logic circuits," *Proceedings of the 18th International Symposium on Multiple-Valued Logic*, May 1988, pp. 21-30.

J. T. Butler and H. G. Kerkhoff, "Multiple-valued CCD circuits," *Computer*, Vol. 21, No. 24, pp. 58-69, April 1988.

J. T. Butler and H. G. Kerkhoff, "Analysis of input and output configurations for use in four-valued programmable logic arrays," *Proceedings of the IEE-E: Computers and Digital Techniques*, Vol. 134, No. 4, pp. 168-176, July 1987.

J. T. Butler, "Efficient tests for diagnosability in three-valued models of local area networks embedded in a wide area network," *Proceedings of the 16th International Symposium on Multiple-Valued Logic*, May 1986, pp. 128-136.

H. G. Kerkhoff and J. T. Butler, "Design of a high-radix programmable logic array using profiled peristaltic charge-coupled devices," *Proceedings of the 16th International Symposium on Multiple-Valued Logic*, May 1986, pp. 100-103 (received Outstanding Contributed Paper Award of the 16th International Symposium on Multiple-Valued Logic).

K. A. Schueller, P. Tirumalai, and J. T. Butler, "Analysis of the cost-table approach to the design of multiple-valued circuits," *Proceedings of the 1986 International Symposium on Multiple-Valued Logic*, May 1986, pp. 42-50.

E. A. Bender and J. T. Butler and H. G. Kerkhoff, "Comparing the SUM with the MAX for use in four-valued PLA's," *Proceedings of the 15th International Symposium on Multiple-Valued Logic*, May 1985, pp. 30-35.

R. A. Leonetti and J. T. Butler, "Characterization of diagnosability of systems with four-valued test results," *Proceedings of the 1986 International Symposium on Multiple-Valued Logic*, May 1985, pp. 52-56 (received Award for Excellence from the Multiple-Valued Logic Technical Committee).

E. A. Bender and J. T. Butler, "Enumeration of structured flowcharts," *Journal of the Associated for Computing Machinery*, pp. 537-548, July 1985.

P. Tirumalai and J. T. Butler, "On the realization of multiple-valued logic functions using CCD PLA's," *Proceedings of the 14th International Symposium on Multiple-Valued Logic*, May 1984, pp. 33-42.

J. T. Butler, "On the number of locations required in the content-addressable memory implementation of multiple-valued functions," *Proceedings of the 13th International Symposium on Multiple-Valued Logic*, May 1983, pp. 94-102.

J.-k. Lee and J. T. Butler, "Tabular methods for the design of CCD multiple-valued circuits," *Proceedings of the 13th International Symposium on Multiple-Valued Logic*, May 1983, pp. 162-171.

J. T. Butler, "Relations among systems diagnosis models with three-valued test outcomes," *Proceedings of the 13th International Symposium on Multiple-Valued Logic*, May 1983, pp. 350-355.

J. T. Butler, "On the relationship between propagating context-dependent Lindenmayer systems and cellular automata systems," *Information Sciences*, pp. 63-67, 1982.

J. T. Butler, "Diagnosis of intermittently faulty and permanently faulty processors in a multiprocessing system using three-valued functions," *Proceedings of the 12th International Symposium on Multiple-Valued Logic*, May 1982, pp. 122-128 (also appears summarized in *Proceedings of COMPCON*, Fall 1982, pp. 145-148).

J. T. Butler, "Speed-efficiency-complexity tradeoffs in universal diagnosis algorithms," *IEEE Transactions on Computers*, C-30, pp. 590-596, August 1981.

J. T. Butler, "Properties of three-valued system diagnosis," *Proceedings of the 11th International Symposium on Multiple-Valued Logic*, May 1981, pp. 85-89.

P. E. White and J. T. Butler, "Synthesis of one-dimensional scope-2 flexible cellular automata systems from input-output configuration pairs," *Information and Control*, 43, pp. 304-326, December 1979.

E. A. Bender and J. T. Butler, "Enumeration of functions realized by fanout-free networks of general multivalued gates," *Proceedings of the 9th International Symposium on Multiple-Valued Logic*, May 1979, pp. 94-103.

J. A. Ginzer and J. T. Butler, "Multiple-valued logic: 1974 - 1978 survey and analysis," *Proceedings of the 9th International Symposium on Multiple-Valued Logic*, May 1979, pp. 1-13.

J. T. Butler, "Synthesis of one-dimensional binary cellular automata systems from composite local maps," *Information and Control*, 43, pp. 304-326, December 1979.

J. T. Butler, "Decomposable maps in general tessellation structures," *Journal of Computer and Systems Sciences*, Vol. 18, no. 1, pp. 1-7, February 1979.

E. A. Bender and J. T. Butler, "Asymptotic approximations for the number of fanout-free functions," *IEEE Transactions on Computers*, C-27, pp. 1180-1183, December 1978.

J. T. Butler, "Tandem networks of universal cells," *IEEE Transactions on Computers*, C-27, pp. 785-800, September 1978.

J. T. Butler, "Analysis and design of fanout-free networks of positive symmetric gates," *Journal of the Association for Computing Machinery*, vol. 24, pp. 481-498, July 1978.

J. T. Butler and S. C. Ntafos, "The vector string descriptor as a tool in the analysis of cellular automata systems," *Mathematical Biosciences*, vol. 35, pp. 55-84, 1977.

J. T. Butler, "Fanout-free networks of multi-valued gates," *Proceedings of the 7th International Symposium on Multiple-Valued Logic*, May 1977, pp. 36-46.

J. T. Butler, "Restricted cellular networks," *IEEE Transactions on Computers*, C-25, pp. 1139-1142, November 1976.

J. T. Butler, "On the number of functions realized by cascades and disjunctive networks," *IEEE Transactions on Computers*, C-24, pp. 681-690, July 1975.

J. T. Butler, "A note on cellular automata complexity tradeoffs," *Information and Control*, 26, pp. 286-295, November 1974.

J. T. Butler and K. J. Breeding, "Some characteristics of universal cell nets," *IEEE Transactions on Computers*, C-22, pp. 897-903, October 1973.

Text and Chapter of a Text

J. T. Butler, "Multiple-Valued Logic in VLSI," Technology Series Text of the *Computer Society Press*, June 1991. This is a reference text consisting of a tutorial introduction, an annotated bibliography, and reprints of twelve papers.

J. T. Butler, "Multiprocessor system diagnosis with three-valued test outcomes," Chapter 18 of Rine, D. C. - *Computer Science and Multiple-Valued Logic: Theory and Applications*, North-Holland Publishing Co., 1984. This is a combination of two manuscripts above.

Unrefereed Contributions

J. T. Butler and T. Sasao, "Redundant multiple-valued number systems," *The Proc. of the Japan Research Group on Multiple-Valued Logic*, Vol. 20, July 1997, pp. 14-1 - 14.8.

J. T. Butler and T. Sasao, "Transition properties of logic functions," The Institute of Electronics, Information, and Communications Engineers, *Technical Report of the IEICS*, February 13, 1997.

T. Sasao and J. T. Butler, "On bi-decompositions of logic functions" *Information Processing Society of Japan Notes*, Vol. 96, No. 121, December 12, 1996, pp. 9-16.

J. T. Butler "Research on multiple-valued logic at the Naval Postgraduate School," *Naval Research Reviews*, Vol. XLIV/XLV, Four/1992 One/1993, pp. 1-8.

T. Sasao and J. T. Butler, "On the analysis of an FPGA architecture," *International Symposium on Information Sciences: Logic synthesis and microprocessor architecture*, pp. 162-168, July 1992.

G. W. Dueck, R. C. Earle, P. T. Tirumalai, and J. T. Butler, "Multiple-valued programmable logic array minimization by simulated annealing," Naval Postgraduate School Technical Report NPS-EC-92-004, Feb. 1992 (extended version of a manuscript above).

K. A. Schueller and J. T. Butler, "The cost-table problem is NP-complete," *Proceedings of the 28th Annual Allerton Conference on Communication, Control, and Computing*, Sept. 1988, regular (full) paper, pp. 948-957.

J. M. Yurchak and J. T. Butler, "HAMLET user reference manual," Naval Postgraduate School Technical Report NPS-6290-015, July 1990.

J. T. Butler and Y. Rosen "Properties of c-correctability in self-diagnosing systems", *Proceedings of the 26th Annual Allerton Conference on Communication, Control, and Computing*, Sept. 1988, regular (full) paper, pp. 408-416.